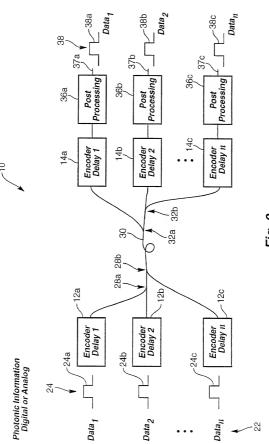
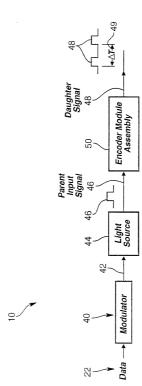


FIG. 1

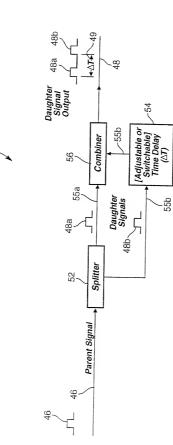


-ig. 2



Differential Delay Multiplexer Sender/Encoder

Fig. 3

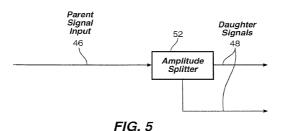


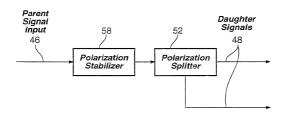
Differential Delay Multiplexer (DDM) Sender/Encoder

Fig. 4

- 1- 1 1

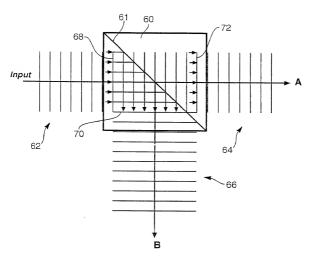
COORDINEY DATED





**Splitting Criteria** 

FIG. 6



Amplitude or Polarization Splitter

FIG. 7

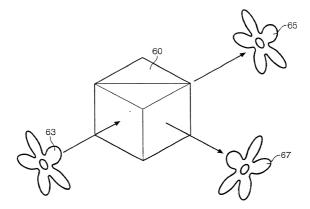
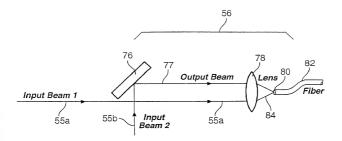


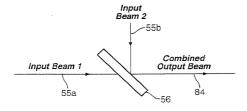
Image Signals Which Maintain Spatial Information

FIG. 7A



Beam Combiner

FIG. 8



Amplitude or Polarization Combiner

FIG. 9

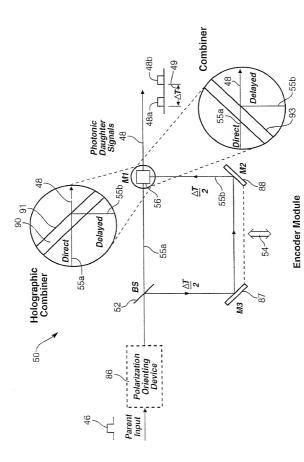
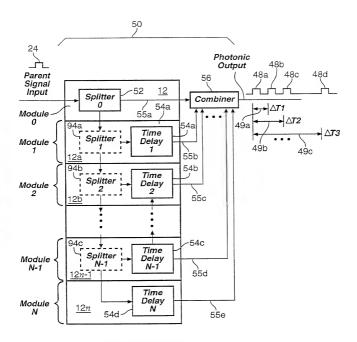


Fig. 10



Composite Encoder Module Assembly

FIG. 11

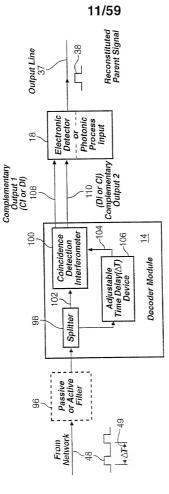


Fig. 12

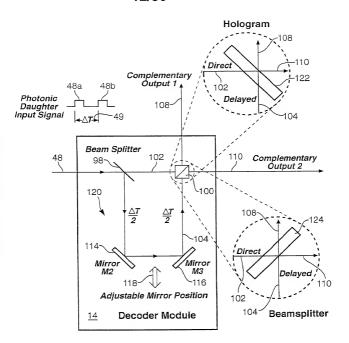


FIG. 13

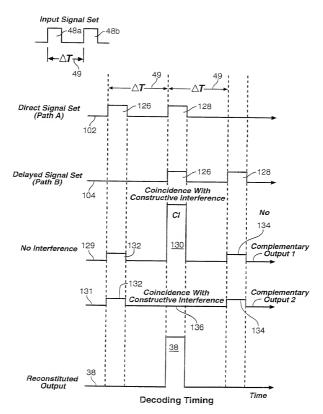


FIG. 14



- 48

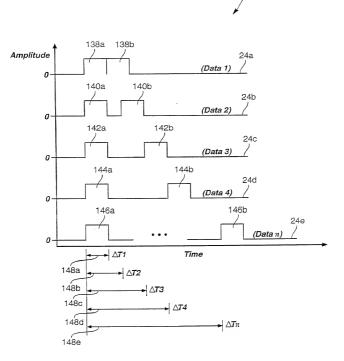


Fig. 15

DE 4 RD 4

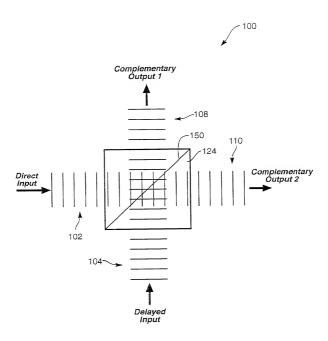


Fig. 16

1 351301

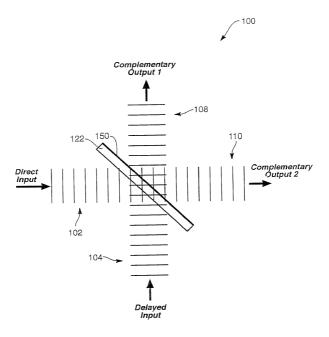


Fig. 17

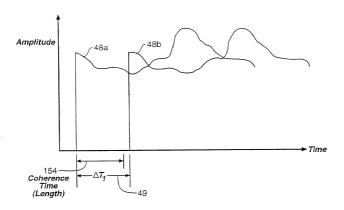


Fig. 18

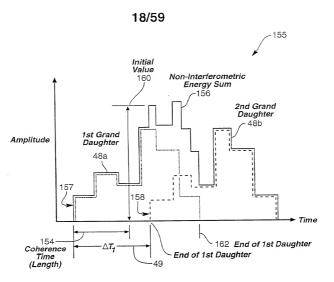


Fig. 19

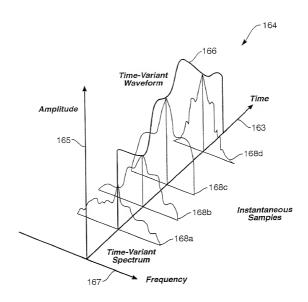
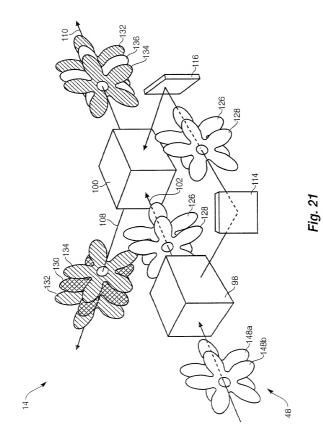
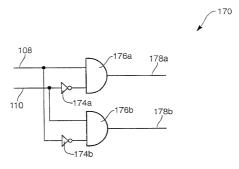
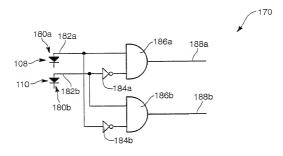


Fig. 20



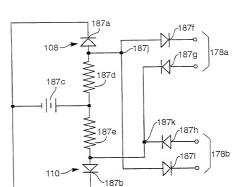


Photonic Processor Fig. 22



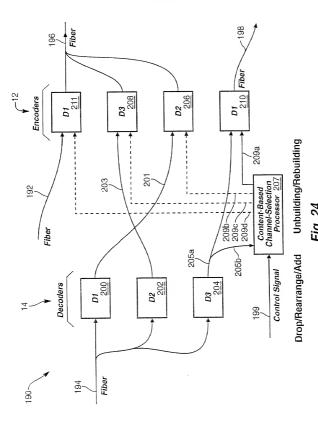
**Electronic Processor** 

Fig. 23A

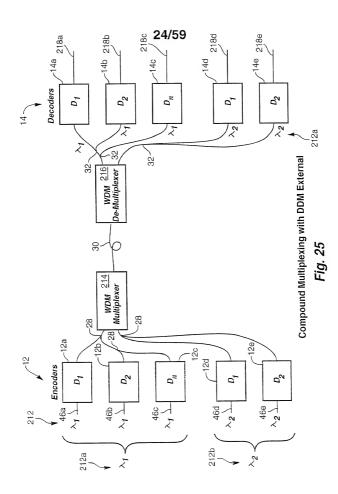


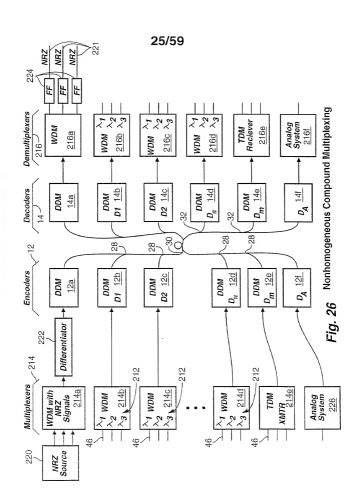
- 170

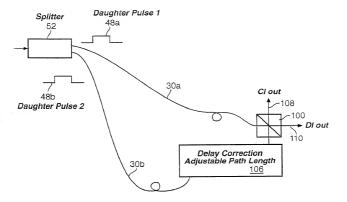
Electronic Processor Fig. 23B



TOUSIES BETTE





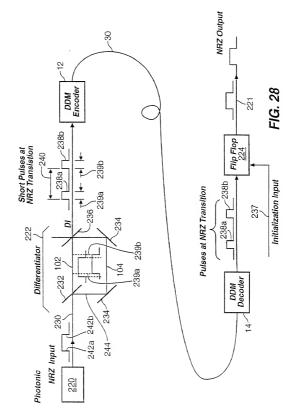


Multiple Delay Path

Integrated Delay and Delay Correction

FIG. 27

Photonic NRZ Interface



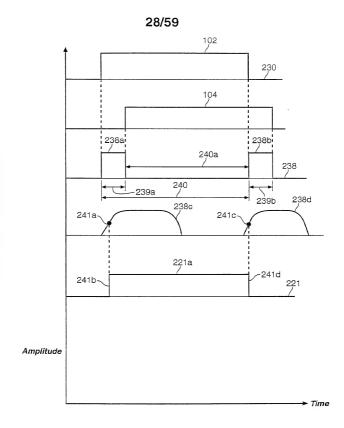
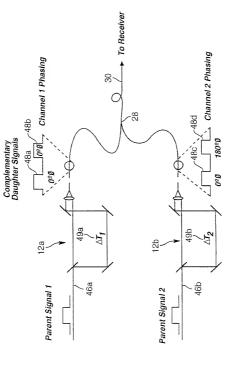


FIG. 29



Phase Sequenced Dual Channel Encoder

FIG. 30

Phase Sequenced Dual Channel Decoder

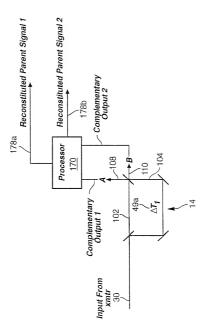


FIG. 31

### Phase Sequence Timing

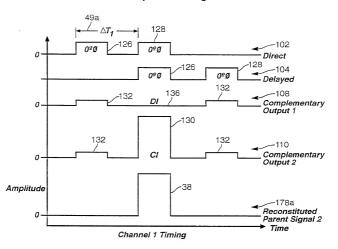


FIG. 32

### **Phase Sequence Timing**

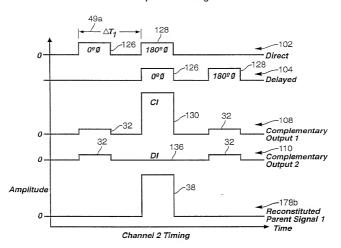
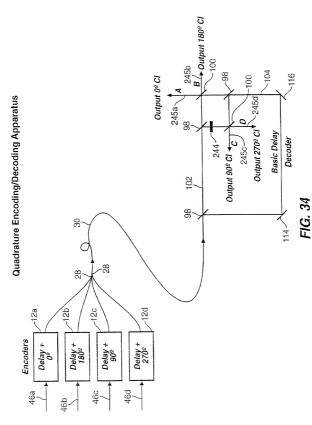


FIG. 33



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46a	Phase of Direct Signal	Phase of Delayed Signal	Quad A	iratur B	re Outputs C D
Channel 1	О	О	CI	DI	C = D
Channel 2	О	180	DI	CI	C = D
Channel 3	О	90	A =	В	CI DI
Channel 4	О	270	A =	В	DI CI
			245a	245b	245c 245d

FIG. 35

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Quadrature Wave Forms For One Channel

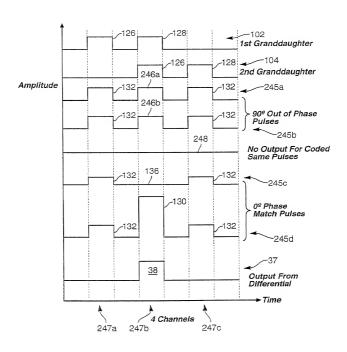


FIG. 36

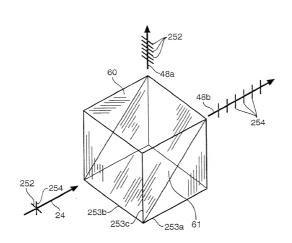


FIG. 37A

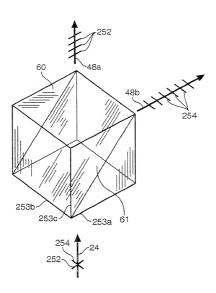
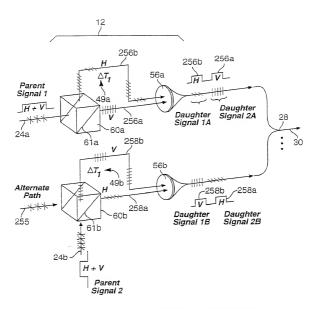
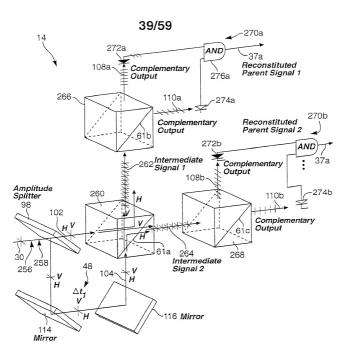


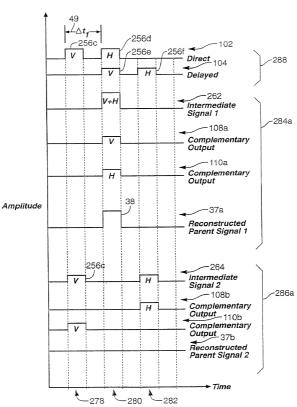
FIG. 37B



Double Encoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Double Decoder With Polarizations Sequenced to Differentiate 2 Channels Having the Same Time Delay Between Daughter Signals



Polarization Sequenced Channel 1 Timing FIG. 40

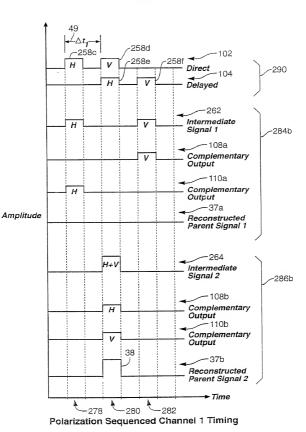
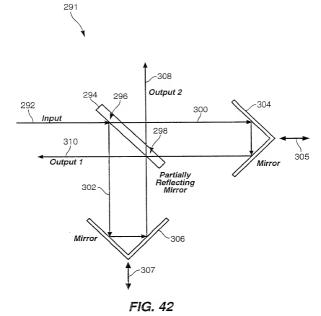


FIG. 41



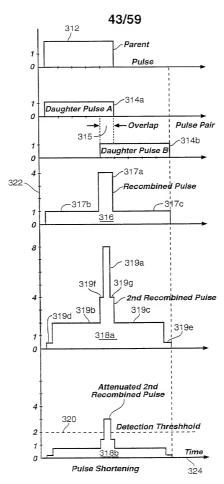


FIG. 43

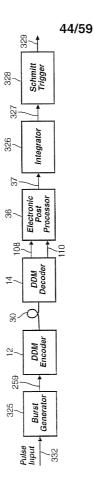


FIG. 44

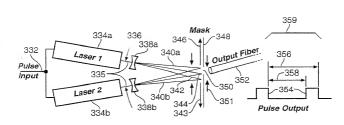
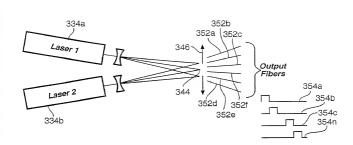


FIG. 45



THE THE

FIG. 46

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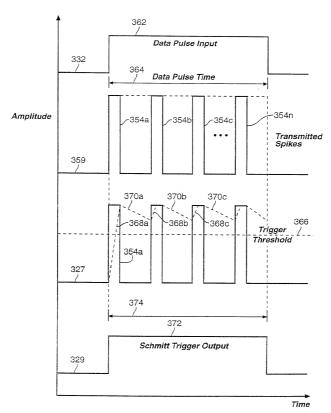


FIG. 47

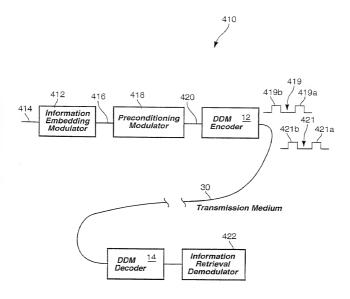
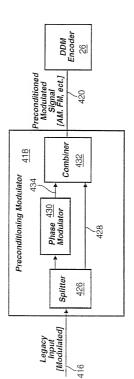


FIG. 48



OCCURCA OUTS

FIG. 49

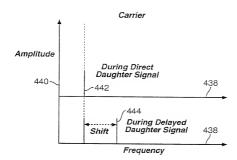
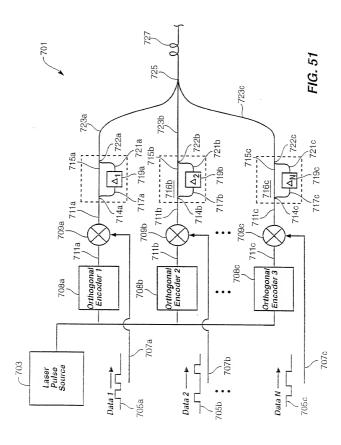


FIG. 50



FORD SEEL DES DES

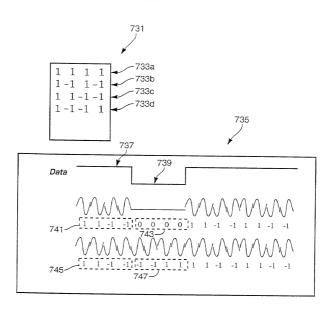
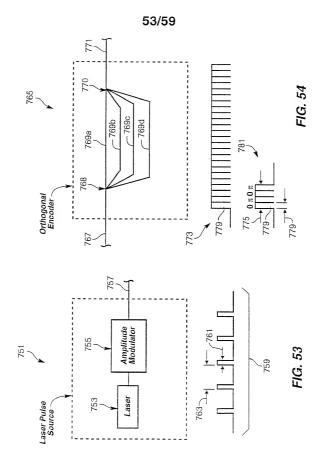
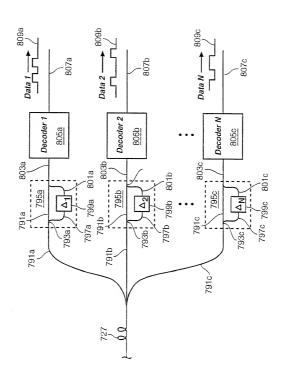
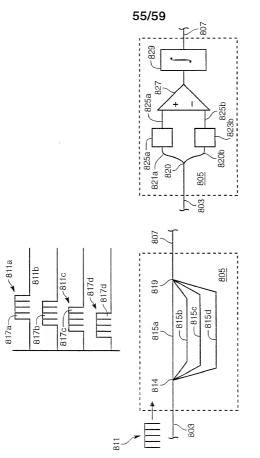


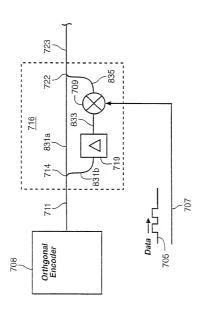
FIG. 52

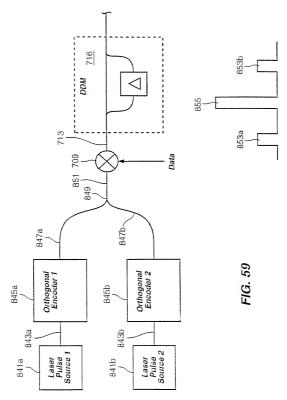






G. 56





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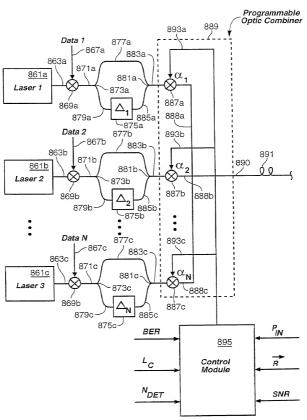


FIG. 60

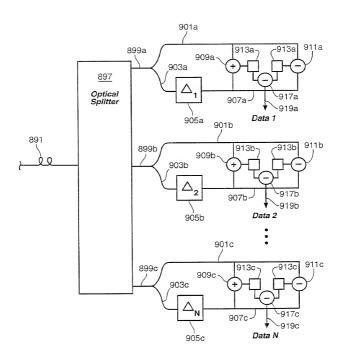


FIG. 61